Non-Volatile SRAM MODULE 16Mbyte (4,096K x 32Bit), PCI interface, (SMM) 5V
Part No. HMNP16MM

GENERAL DESCRIPTION

The HMNP16MM Nonvolatile SRAM is a 16,777,216-byte static RAM organized as 8,388,608 words by 16 bits. The HMNP16MM has a self-contained lithium energy source provide reliable non-volatility coupled with the unlimited write cycles of standard SRAM and integral control circuitry which constantly monitors the single 5V supply for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on to sustain the memory until after V_{CC} returns valid and write protection is unconditionally enabled to prevent garbled data.

In addition the SRAM is unconditionally write-protected to prevent an inadvertent write operation. At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The HMNP16MM uses extremely low standby current CMOS SRAM's, coupled with small lithium coin cells to provide non-volatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

FEATURES

- Access time : 70, 85 and 100ns
- High-density design : 16Mbyte Design
- Battery internally isolated until power is applied
- Unlimited write cycles
- Data retention in the absence of V_{CC}
- 10-years minimum data retention in absence of power
- Automatic write-protection during power-up/power-down cycles
- Data is automatically protected during power loss
- Industrial temperature operation

OPTIONS MARKING

- Timing

70 ns	- 70
85 ns	- 85
100 ns	-100

PIN ASSIGNMENT

P1				P2			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	NC	2	TRST*	1	TCK	2	NC
3	TMS	4	TDO	3	GND	4	INTA*
5	TDI	6	GND	5	INTB*	6	INTC*
7	GND	8	NC	7	NC	8	VCC
9	NC	10	NC	9	INTD*	10	NC
11	NC	12	NC	11	GND	12	NC
13	P_RST*	14	NC	13	P_CLK	14	GND
15	NC	16	NC	15	GND	16	P_GNT*
17	NC	18	GND	17	P_REQ*	18	VCC
19	P_AD(30)	20	P_AD(29)	19	NC	20	P_AD(31)
21	GND	22	P_AD(26)	21	P_AD(28)	22	P_AD(27)
23	P_AD(24)	24	NC	23	P_AD(25)	24	GND
25	P_IDSEL	26	P_AD(23)	25	GND	26	P_C_BE3*
27	NC	28	P_AD(20)	27	P_AD(22)	28	P_AD(21)
29	P_AD(18)	30	GND	29	P_AD(19)	30	VCC
31	P_AD(16)	32	P_C_BE2*	31	NC	32	P_AD(17)
33	GND	34	NC	33	P_FRAME*	34	GND
35	P_TRDY*	36	NC	35	GND	36	P_IRDY*
37	GND	38	P_STOP*	37	P_DEVSEL*	38	VCC
39	P_PERR*	40	GND	39	GND	40	P_LOCK*
41	NC	42	P_SERR*	41	NC	42	NC
43	P_C_BE1*	44	GND	43	P_PAR	44	GND
45	P_AD(14)	46	P_AD(13)	45	NC	46	P_AD(15)
47	GND	48	P_AD(10)	47	P_AD(12)	48	P_AD(11)
49	P_AD(8)	50	NC	49	P_AD(9)	50	VCC
51	P_AD(7)	52	NC	51	GND	52	P_C_BE0*
53	NC	54	NC	53	P_AD(6)	54	P_AD(5)
55	NC	56	GND	55	P_AD(4)	56	GND
57	NC	58	NC	57	NC	58	P_AD(3)
59	GND	60	NC	59	P_AD(2)	60	P_AD(1)
61	ACK64*	62	NC	61	P_AD(0)	62	VCC
63	GND	64	NC	63	GND	64	REQ64*

FUNCTIONAL DESCRIPTION

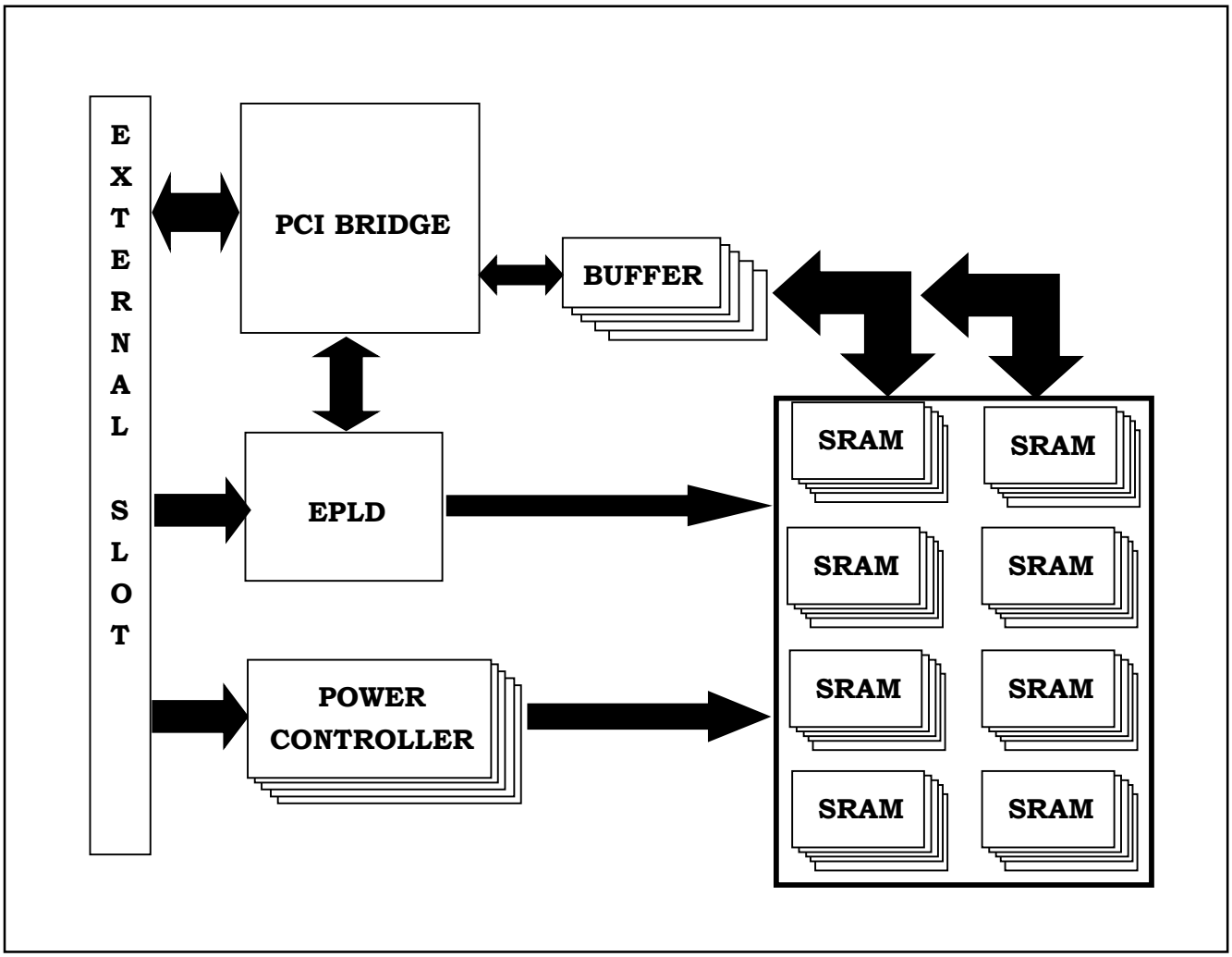
The HMNP16MM executes a read cycle whenever /WE is inactive(high) and /CE is active(low). The address specified by the address inputs(A_0-A_{19}) defines which of the 16,777,216 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (access time) after the last address input signal is stable.

When power is valid, the HMNP16MM operates as a standard CMOS SRAM. During power-down and power-up cycles, the HMNP16MM acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

The HMNP16MM is in the write mode whenever the /WE and /CE signals are in the active (low) state after address inputs are stable. The later occurring falling edge of /CE or /WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of /CE or /WE. All address inputs must be kept valid throughout the write cycle. /WE must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The /OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus been enabled (/CE and /OE active) then /WE will disable the outputs in t_{ODW} from its falling edge.

The HMNP16MM provides full functional capability for Vcc greater than 4.5 V and write protects by 4.37 V nominal. Power-down/power-up control circuitry constantly monitors the Vcc supply for a power-fail-detect threshold V_{PFD}. When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All inputs to the RAM become “don’t care” and all outputs are high impedance. As Vcc falls below approximately 3 V, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when Vcc rises above approximately 3.0 volts, the power switching circuit connects external Vcc to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after Vcc exceeds 4.5 volts.

BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	I/O OPERATION	POWER
Not selected	X	H	X	High Z	Standby
Output disable	H	L	H	High Z	Active
Read	L	L	H	D_{OUT}	Active
Write	X	L	L	D_{IN}	Active

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	REMARK
Voltage on any pin relative to Vss	Vin,V_{CC}	-0.5 to 7.0	V	
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	
Power Dissipation	Pd	32	W	
Storage temperature	T_{STG}	-65 to 150	°C	
Operating Temperature	Ta	0 to 70	°C	K6T4016C3C-B
		-40 to 85	°C	K6T4016C3C-F

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to the Recommended DC Operating Conditions detailed in this data sheet.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS ($T_A = T_{OPR}$)

PARAMETER	SYMBOL	MIN	TYPICAL	MAX
Supply Voltage	V_{CC}	4.5V	5.0V	5.5V
Ground	V_{SS}	0	0	0
Input high voltage	V_{IH}	2.2	-	V_{CC}+0.5V
Input low voltage	V_{IL}	-0.5	-	0.8V

NOTE: Typical values indicate operation at T_A = 25℃

DC AND OPERATING CHARACTERISTICS (T_A= T_{OPR}, V_{CCmin} ≤ V_{CC}≤ V_{CCmax})

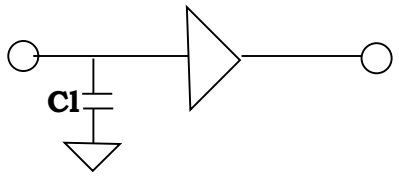
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Input Leakage Current	V_{IN}=V_{SS} to V_{CC}	I_{LI}	-1	-	1	μA
Output Leakage Current	/CE=V_{IH} or /OE=V_{IH} or /WE=V_{IL}	I_{LO}	-1	-	1	μA
Output high voltage	I_{OH}=-1.0mA	V_{OH}	2.4	-	-	V
Output low voltage	I_{OL}= 2.1mA	V_{OL}	-	-	0.4	V
Standby supply current(TTL)	/CE=$V_{IH,}$ Other input = Vil or Vih	I_{SB}	-		3	mA
Standby supply current(CMOS)	/CE≥V_{CC}-0.2V, Other inputs = 0 ~ Vcc	I_{SB1}	-		20	μA
Operating supply current	Min.cycle,duty=100%, /CE=V_{IL}, $I_{I/O}$=0mA, A_{19}<V_{IL} or A_{19}>V_{IH} A_{20}<V_{IL} or A_{20}>V_{IH}	I_{CC}	-		10	mA

CAPACITANCE (T_A=25℃, f=1MHz, V_{CC}=5.0V)

DESCRIPTION	CONDITIONS	SYMBOL	MAX	MIN	UNIT
Input Capacitance	Input voltage = 0V	C_{IN}	8	-	pF
Input/Output Capacitance	Output voltage = 0V	$C_{I/O}$	10	-	pF

AC CHARACTERISTICS (Test Conditions)

PARAMETER	VALUE
Input pulse levels	0 to 2.4V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5V (unless otherwise specified)
Output load (including scope and jig)	See rignt



Cl = 100pF + 1TTL

50pF + 1TTL

READ CYCLE (T_A= T_{OPR}, V_{CCmin} ≤ V_{CC}≤ V_{CCmax})

PARAMETER	SYMBOL	55 ns		70 ns		UNIT
		Min	Max	MIN	MAX	
Read Cycle Time	t_{RC}	55		70	-	Ns
Address Access Time	t_{ACC}		55	-	70	Ns
Chip enable access time	t_{ACE}		55	-	70	Ns
Output enable to Output valid	t_{OE}		25	-	35	Ns
Chip enable to output in low Z	t_{CLZ}	5		5	-	ns
Output enable to output in low Z	t_{OLZ}	5		5	-	ns
Chip disable to output in high Z	t_{CHZ}	0	20	0	25	ns
Output disable to output high Z	t_{OHZ}	0	20	0	25	ns
Output hold from address change	t_{OH}	10		10	-	ns

WRITE CYCLE (T_A= T_{OPR}, V_{CCmin} ≤ V_{CC} ≤ V_{CCmax})

PARAMETER	SYMBOL	50 ns		70ns		UNIT
		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	55		70	-	ns
Chip enable to end of write	t_{CW}	45		60	-	ns
Address setup time	t_{AS}	0		0	-	ns
Address valid to end of write	t_{AW}	45		60	-	ns
Write pulse width	t_{WP}	45		55	-	ns
Write recovery time	t_{WR1}	0		0	-	ns
Write to output high-Z	t_{DW}	0	20	0	25-	ns
Data to writer time overlap	t_{DH1}	25		30	-	ns
Data hold from write time	t_{DH2}	0		0	-	ns
End write to output low-Z	t_{WZ}	5		5		ns
/LB, /UB valid to end of write	t_{OW}	45		60	-	ns

NOTE: 1. A write ends at the earlier transition of /CE going high and /WE going high.

2. A write occurs during the overlap of allow /CE and a low /WE. A write begins at the later transition of

/CE going low and /WE going low.

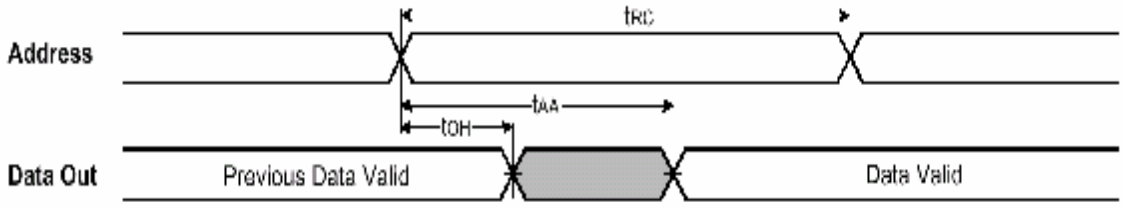
3. Either t_{WR1} or t_{WR2} must be met.

4. Either t_{DH1} or t_{DH2} must be met.
5. If /CE goes low simultaneously with /WE going low or after /WE going low, the outputs remain in high-impedance state.

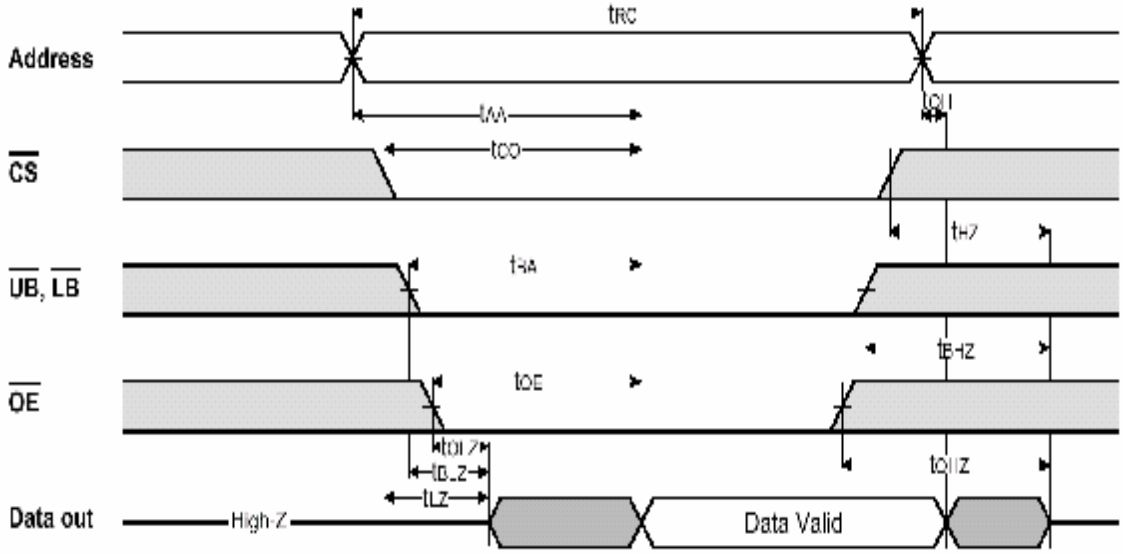
TIMING WAVEFORM

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



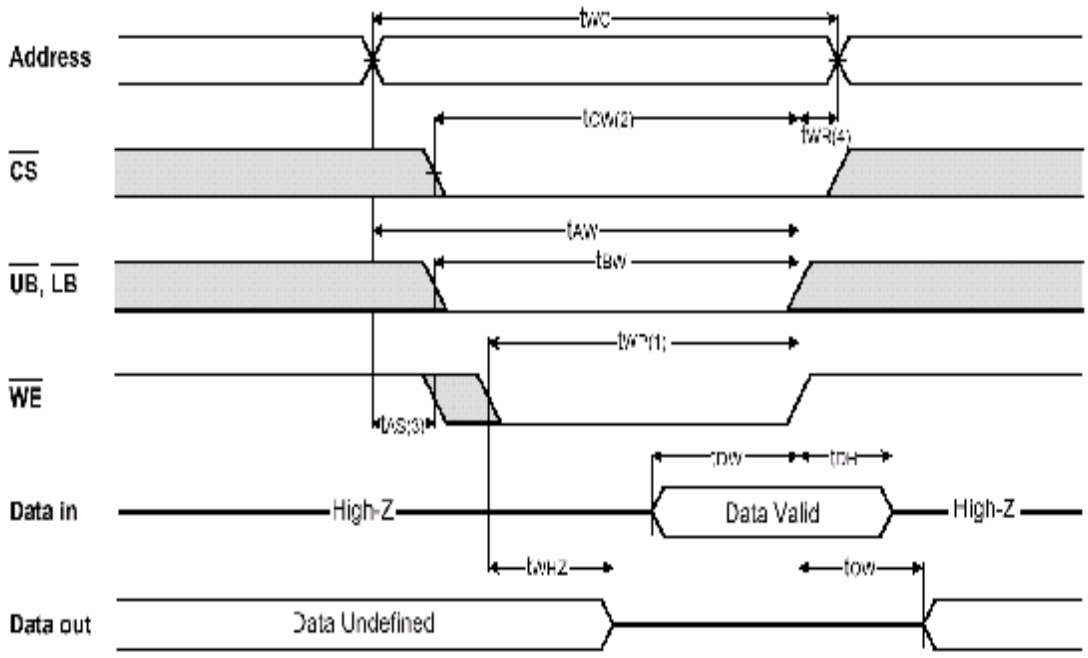
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



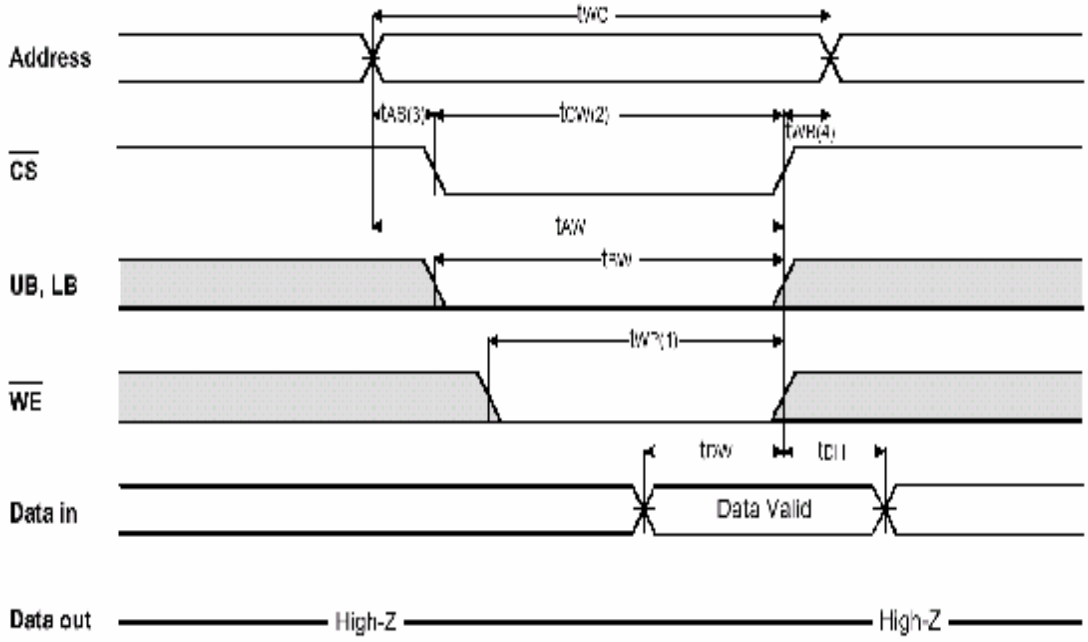
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

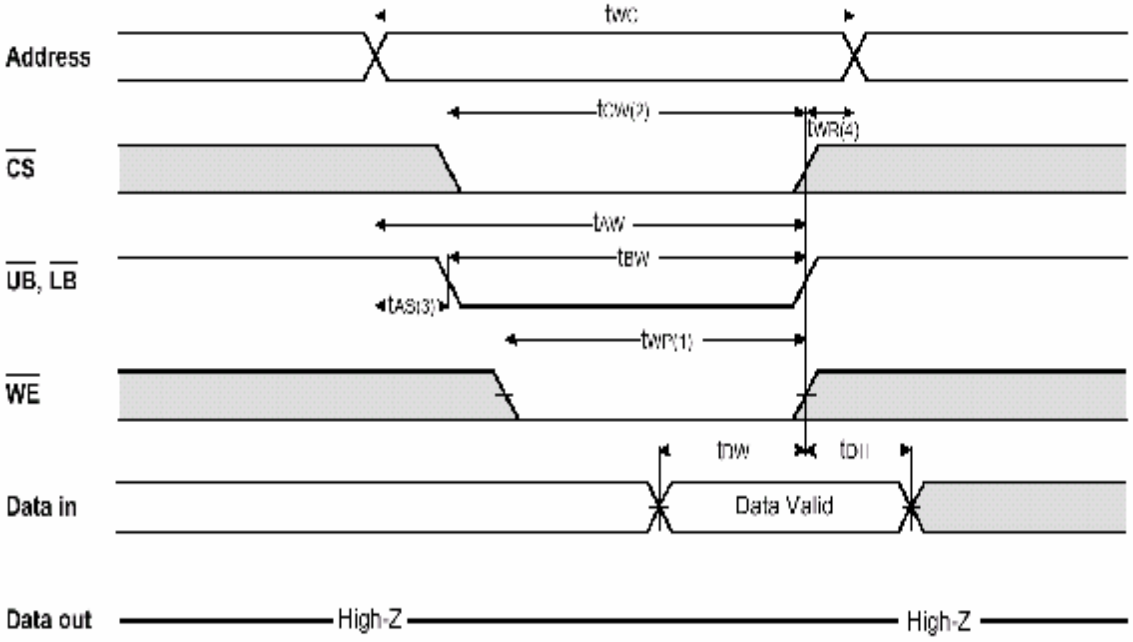
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

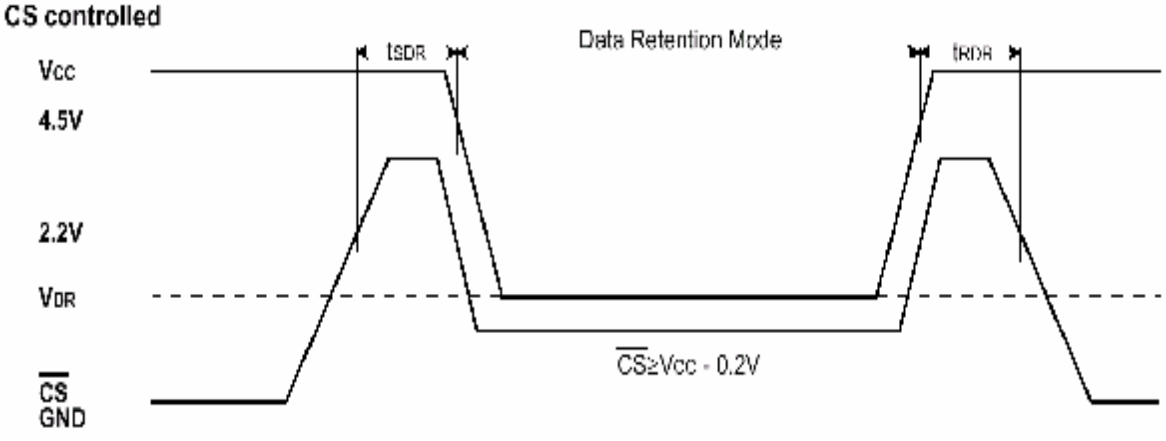


NOTES (WRITE CYCLE)

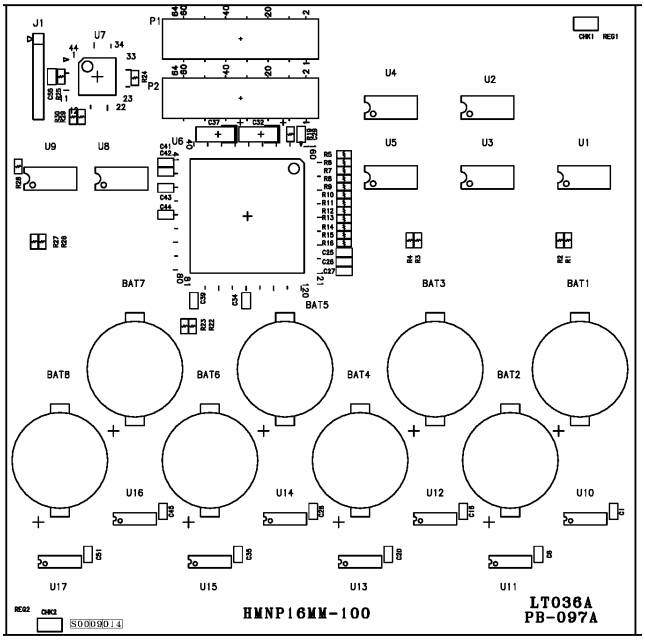
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

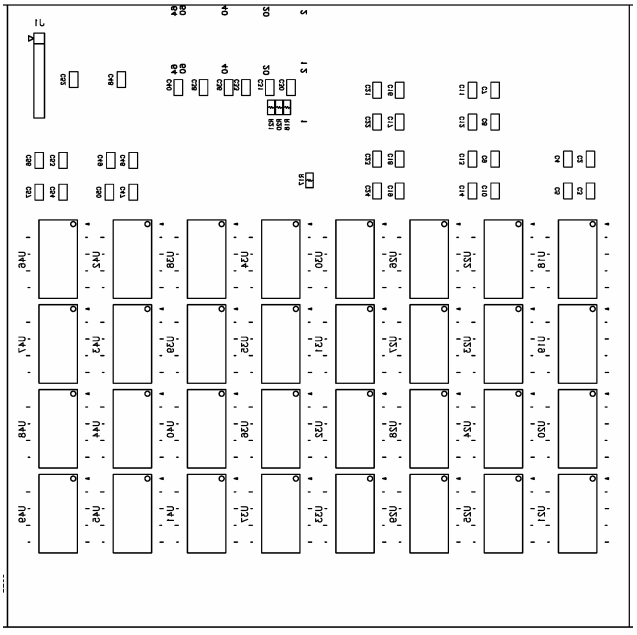
$\overline{CS}$ controlled



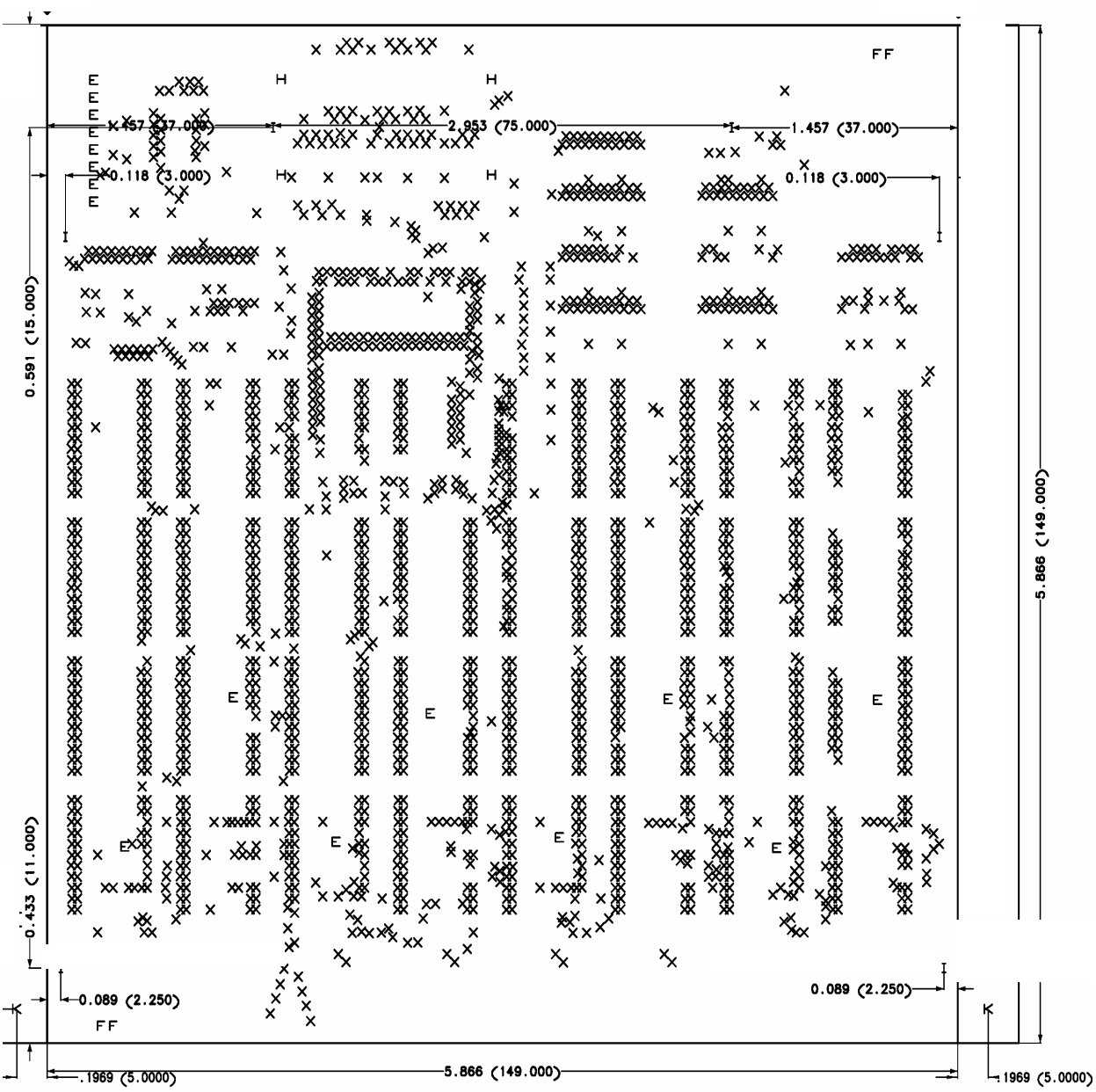
PACKAGE DIMENSION



<FRONT VIEW>



<REAR VIWE>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0.591 (15.000)
0.433 (11.000)
5.866 (149.000)
0.089 (2.250)
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.1969 (5.0000)

ORDERING INFORMATION

Part Number	Density	Org.	Package	Vcc	Component number	Speed
HMNP16MM-100	16Mbyte	x 32	128 Pin-MMC	5V	32 EA	100ns